ABSTRACT OF THE DISCLOSURE

An intervote modulator (10) includes a majority voting logic unit (12) and an interplex modulator (14). The majority voting logic unit receives plural signal codes (e.g., five codes x_1, x_2, x_3, x_4, x_5) together with their respective target gains G_1, G_2, G_3, G_4, G_5 representing the desired transmit power for the individual signal codes. The majority voting logic unit combines three of these five signal codes to form a majority vote composite signal while keeping the other two signal codes uncombined. The majority vote composite signal and the two uncombined signals are then supplied to the interplex modulator as signals s_1, s_2 and s_3. The interplex modulator applies interplex modulation to signals s_1, s_2 and s_3 to form the in-phase and quadrature components of the final composite signal. The majority voting logic unit employs a generalized majority vote involving an interlace of sub-majority votes determined on a chip-by-chip basis.